

## REMARKS/ARGUMENTS

1. In the above referenced Office Action, the Examiner rejected claims 1-5 and 16-18 under 35 USC § 103 (a) as being unpatentable over Hayashi (U.S. Patent No. 6,366,172) in view of Yamaguchi (U.S. Patent No. 6,804,500) and claims 6-15 under 35 USC § 103 (a) as being unpatentable over Hayashi (U.S. Patent No. 6,366,172) in view of Yamaguchi (U.S. Patent No. 6,804,500) further in view of Hans (U.S. Patent No. 5,923,215). The rejections and objections have been traversed and, as such, the applicant respectfully requests reconsideration of the allowability of claims 1-18.
2. Claims 1-5 and 16-18 have been rejected under 35 USC § 103 (a) as being unpatentable over Hayashi (U.S. Patent No. 6,366,172) in view of Yamaguchi (U.S. Patent No. 6,804,500). The applicant respectfully disagrees with the Examiner's arguments supporting this rejection.

The highly linear power amplifier of claim 1 includes a component, a first transistor pair and a second transistor pair. The first transistor pair is coupled in series with the component, wherein a first transistor of the first transistor pair is coupled to receive an input signal and wherein a second transistor of the first transistor pair is coupled to receive a first enable signal. The second transistor pair is coupled in series with the component, wherein a first transistor of the second transistor pair is coupled to receive the input signal, wherein a second transistor of the second transistor pair is coupled to receive a second enable signal, wherein when the first enable signal is enabled the highly linear power amplifier has a first gain with a first linearity and when the second enable signal is enabled the highly linear power amplifier has a second gain with the first linearity.

The combined teachings of Hayashi and Yamaguchi fail to teach or suggest a highly linear power amplifier as is presently claimed in claim 1. For instance, Hayashi teaches an amplifier circuit 1 of figure 1 that includes cascoded transistors 101 and 102. Transistor 102 receives a fixed bias voltage from transistor 400 (column 7, lines 9-10). The amplifier circuit 1 of Hayashi is designed to overcome the negative characteristics of

the output conductance of the cascode amplifier as shown in Figure 9. For example, the improvement means may be either the ON resistance  $R_{ON}$  of the transistor inserted between the fixed voltage  $V_b$  and the gate of transistor 102 or any resistor other than the ON resistor  $R_{ON}$  of the transistor, thereby reducing the Miller effect. (column 7, lines 21-31) As such, Hayashi teaches controlling the impedance of the gate of transistor 102 via transistor 400 or a resistor to reduce the Miller effect, thus enabling the amplifier circuit 1 to be stable at higher operating frequencies than the prior art circuit of Figure 4.

Yamaguchi teaches a power amplifier circuit as shown in Figure 7 that includes an input matching circuit 3i, an input connection unit 2i, a high output amplifier cell block 1a, a low output amplifier cell block 1b, an output connection unit 2o, and an output matching circuit 3o that is more efficient at lower power levels than the disclosed prior art. Figures 9a and 11a illustrate schematic block diagrams of the high output amplifier cell block 1a and figures 9b and 11b illustrate schematic block diagrams of the low output amplifier cell block 1b.

The high output amplifier cell block 1a of Figure 9a includes two amplifiers cells that are coupled in parallel to receive an input  $IN_a$  and to produce an output  $OUT_a$ . Further, the amplifier cells 4a and 4b are coupled in parallel to a control signal  $V_{cnta}$  and to a power source  $V_{dca}$ . The low output amplifier cell block 1b of Figure 9b includes two amplifier cells 4c and 4d and an AC/DC separation unit 5. The AC/DC separation unit 5 functions to divide the supply voltage to the amplifier cells 4c and 4d in half. (column 8, lines 31-36) By dividing the supply voltage in half, the maximum output power is reduced by  $\frac{1}{4}$ . (column 8, lines 45-48) Thus, for low output power applications, the low output amplifier cell block 1b is enabled and the high output amplifier cell block 1a is disable and the reverse for high output power applications. (column 8, lines 49-60) Figures 12 and 13a-13c illustrate that more than two amplifier cell blocks may be used, where the first [figure 13a] using the full supply voltage, the second [figure 13b] using half of the supply voltage, and the third [figure 13b] using  $\frac{1}{4}$  of the supply voltage.

As such, the reducing of the Miller effect of Hayashi combined with the selectable low output power/high output power amplifier cell blocks of Yamaguchi fail to teach or suggest a highly linear amplifier that includes a component and two transistor pairs as is claimed in claim 1. In particular, the combined references fail to teach or suggest two transistor pairs to provide two different gains for a highly linear power amplifier, where the highly linear power amplifier has the same linearity regardless of which gain is enabled.

Claims 2-5 are dependent upon claim 1 and introduce additional patentable subject matter. The applicant believes that the same reasons that distinguish claim 1 over the present rejection are applicable in distinguishing claims 2-5 over the same rejection.

Claim 16 includes first and second gain limitations and, as such, the applicant believes that the reasons that distinguish claim 1 over the present rejection are applicable in distinguishing claim 16 over the same rejection.

Claims 17 and 18 are dependent upon claim 16 and introduce additional patentable subject matter. The applicant believes that the same reasons that distinguish claim 1 over the present rejection are applicable in distinguishing claims 17 and 18 over the same rejection.

3. Claims 6-15 have been rejected under 35 USC § 103 (a) as being unpatentable over Hayashi (U.S. Patent No. 6,366,172) in view of Yamaguchi (U.S. Patent No. 6,804,500) further in view of Hans (U.S. Patent No. 5,923,215). The applicant respectfully disagrees with the Examiner's arguments supporting this rejection.

Claims 6 and 7 are dependent upon claim 1 and introduce additional patentable subject matter. As demonstrated above, the combined teachings of Hayashi and Yamaguchi fail to teach or suggest the highly linear amplifier of claim 1. Thus, the additional teachings of Hans combined with Hayashi and Yamaguchi still fails to teach

the present highly linear amplifier. As such, the applicant believes that claims 6 and 7 overcome the present rejection.

Claim 8 includes similar limitations as claim 1 with respect to first and second gains and linearity. As demonstrated above, the combined teachings of Hayashi and Yamaguchi fail to teach or suggest the highly linear amplifier of claim 1. Thus, the additional teachings of Hans combined with Hayashi and Yamaguchi still fails to teach the present highly linear amplifier. As such, the applicant believes that claim 8 overcomes the present rejection.

Claims 9-11 are dependent upon claim 8 and introduce additional patentable subject matter. The applicant believes that the same reasons that distinguish claim 8 over the present rejection are applicable in distinguishing claims 9-11 over the same rejection.

Claim 12 includes similar limitations as claim 1 with respect to first and second gains and linearity. As demonstrated above, the combined teachings of Hayashi and Yamaguchi fail to teach or suggest the highly linear amplifier of claim 1. Thus, the additional teachings of Hans combined with Hayashi and Yamaguchi still fails to teach the present highly linear amplifier. As such, the applicant believes that claim 12 overcomes the present rejection.

Claims 13-15 are dependent upon claim 8 and introduce additional patentable subject matter. The applicant believes that the same reasons that distinguish claim 8 over the present rejection are applicable in distinguishing claims 13-15 over the same rejection.

For the foregoing reasons, the applicant believes that claims 1-18 are in condition for allowance and respectfully request that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.

RESPECTFULLY SUBMITTED,

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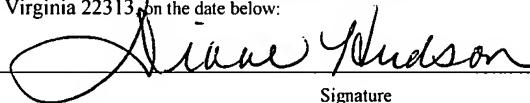
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